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# Nanorelays- Power Driver of the Next Decade

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**Abstract.** The exploding market of portable electronic appliances has fuelled the demand for complex integrated systems that can be run by light weight batteries with long shelf life. But as technology continued to scale, leakage power has proven to be a dominant source of power dissipation. Looking beyond the Complementary Metal-Oxide Semiconductor (CMOS) transistor, this paper presents an unexplored alternative-the Nanorelay that can potentially eradicate the foreseen crisis in the IC era. By using modern CMOS processes the relay can get a microscopic makeover which can lead to further advances in power reduction as these devices posses "green–switch" properties like zero leakage current, infinite sub-threshold slope and temperature resilient behavior and are hence ideal candidates for ultra low-power (ULP) chips that can run of scavenged energy from light, acoustic vibrations or ambient RF signals and primarily for realizing programmable switches in FPGAs. Power consumption is a key issue in the design of portable systems such as smart cards, pacemakers and defibrillators that posses critical functionality. These systems rely on embedded batteries as their source of power which has limited life. Increased power consumption leads to increased battery size and an increase in product size and weight. Henceforth, methods of reducing power is explored and incorporated.

**Keywords:** Nanorelays, Leakage currents, Power dissipation, CMOS, Pull-in voltage, Delay, FPGA.

## 1. Introduction

CMOS integrated circuit (IC) technology has lead to tremendous development in data storage, computation and processing over the past three decades. However, as the demand for miniaturized electronic devices grew, the energy consumption and power dissipation for the sub-nanometer CMOS ICs increased drastically due to various second order effects like: sub-threshold leakage, hot carriers injection, die processes, short channel and drain punch-through effects caused by thermal variations [1].The chip industry is fast approaching a crisis as continued improvement in energy efficiency has begun to stall thus invoking the immediate need for an alternative device or methodology. The future now lies in the past – looking back to the yester years of electrically driven computing, there emerges the electrostatically actuated Nano-Electro-Mechanical Relay (NEMS) or simply Nanorelays. These devices posses extremely low on-state resistance (≈0.5Ω) and infinitely large off-state resistance i.e. Virtually zero leakage currents and are hence ideal for ultralow-power (ULP) chips that can run off scavenged energy from light, acoustic vibrations or ambient RF signals. Both lifetime and size of battery powered microelectronic systems are tightly constrained by the energy storage or scavenging device and the node consumption [9]. Significant research effort has been attributed towards aggressively reducing the power requirements, but only a small fraction of the proposed methodologies have been successfully implemented in the current design flows.

## 2. Need For Nanorelays

Conventional transistors are imperfect switches i.e. they leak current even when off. They have a trade off between the transistor operating voltage and the switching time. As threshold voltage is scaled, the off-

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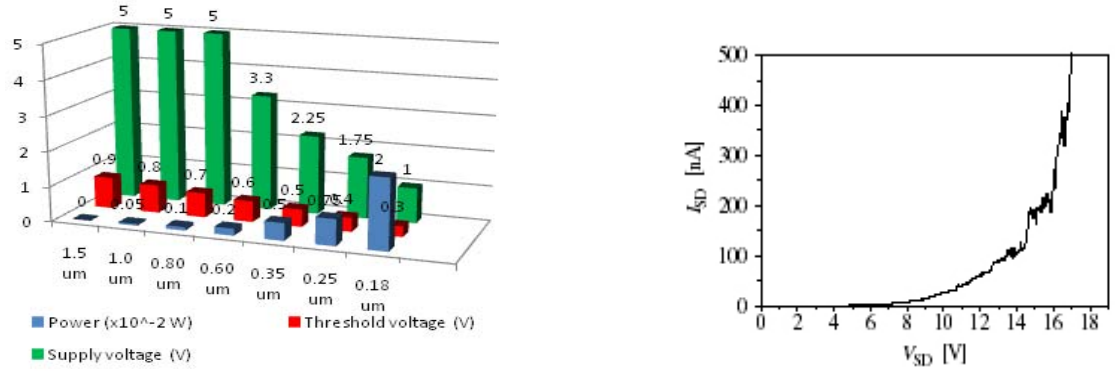
state leakage current increases exponentially. So there is a fundamental limit to the power efficiency of a CMOS circuit and we're fast approaching a near saturation point wherein the primitive technique of simply scaling the transistors won't result in a profound improvement in the chip performance without increasing the power consumption. On the other hand, nano-relays have no leakage currents and they can change states with just a fraction of the energy that's needed to turn a transistor on and off. Sleep transistors are used to reduce leakage power dissipation in multi-threshold CMOS processes. When these devices are used to gate power to the logic blocks, a fundamental trade off arises between the leakage power, dynamic resistance and chip area. The introduction of nano-relays can potentially mitigate majority of the issues involved in using CMOS devices as sleep transistors while greatly boosting the performance and relaxing various constraints. The on-resistance will drop by an order of magnitude, the off- resistance will increase infinitely and the switching thresholds can be maintained [10]. The system clock frequency has scaled at a slower pace but the energy consumption has ballooned to unacceptable levels. NEMS devices offer very low power consumption (< 10μW) and a high shock resistance (>5000GΩ) due to electrostatic actuation. In FPGAs, the traditional use of nmos pass transistors cause signal degradation of logic-high voltages. This demands the need for a level restoring logic (sense inverter) on every wire to compensate for the leakage currents by boosting the signal levels thereby leading to large chip area. Meanwhile, nanorelays pass both logic-low and logic-high as strong signals thus eliminating the need for any level restoring blocks; henceforth saving chip area. The MOSFETs rely on a depleted channel to isolate source and drain which are physically connected through the semiconductor substrate leading to low isolation between the actuation circuit and contact circuit i.e. high off-state capacitance. They are prone to performance degradation due to unwanted harmonics at high operating frequencies as a result of their inherent non-linear power characteristics. In the ON state, they suffer from high insertion and return losses due to high series resistance and impedance mismatch respectively. Nanorelays provide a solution that combines the performance of electromechanical relays with a dimension scale and cost structure of microelectronic devices.




(a). (b)

Fig. 1: (a) Average power consumption trends for Intel MPUs as a function of technology generation [14, 15]; (b) Source-drain current v/s source-drain voltage for a nanorelay (in non-contact mode) with no gate voltage.

From Fig.1, we may observe that average power and hence power density (i.e., power dissipated per unit area) increase as minimum feature size shrinks. This phenomenon has two concomitant causes: (1) Die size has been steadily increasing with technology, causing an increase in total average power. (2) Supply voltage reduction has deviated from the norms of constant-field scaling. Historically, supply voltage scaling has always lagged the device size miniaturization because: (i) Voltage supply levels have been standardized (3.3V, 5V) (ii) Transistor switching frequency can be increased by allowing the electric field to rise in the device (i.e., overdriving the transistor into the saturation region of the transfer curve). This approach is known as 'constant voltage scaling', and it has been adopted in older silicon technologies, upto 0.8 μm.

As shown in Fig.1, supply voltage has started to decrease with shrinking device size even for high-performance transistors [15]. Technology-driven voltage scaling has two major consequences: (1) Aggressively scaled transistors with ultra short channel length tend to become increasingly leaky in the OFF state, and so there is minimal scope for further voltage scaling (2) Multi-threshold techniques that were proposed to facilitate the CMOS devices meet the rigid power constraints lose effectiveness in the sub-

nanometer generation as more transistor switches become timing critical; variable-threshold techniques require stand-by control circuits to even partially address the quiescent leakage problem. Hence the very feature (zero static power dissipation) that made CMOS the mainstream IC technology foresees a major loop hole in the next generation of Pico-devices.

## 3. Design and Fabrication

An electrostatic switch motivated by the CMOS transistor contains a source, drain and a channel through which current flows. The gate and body electrodes control the device's state. The key structural difference is that the gate/channel are suspended above the source/drain rather than built alongside them. This results in less area overhead and minimal cost penalty than their CMOS counterpart. The overall structure offers low insertion loss (<0.1dB), better isolation (>60dB at 6GHz) and excellent linearity than solid state devices. This all-metal structure can be modeled as a low resistance transmission line.

### 3.1. Design and Operation

Fig.2 shows a NEM switch. The switch has a moveable cantilever beam with nickel coated on an oxide layer [1]. The base constitutes the drain, body and source electrodes which are placed adjacent to each other; the body serves as a reference potential for the gate. A thin layer of a conductive material is attached to the insulating underbelly of the gate to form the channel. The gate consisting of a square and four springy suspension coils attached at the corners, is etched out of a conductive Si-Ge alloy and is suspended <100 nm(15 nm) above the 'base'. Let Vgb be the voltage applied between gate and body (cantilever), Vpi be the threshold (pull–in) voltage and Vpo be the pull-out voltage.

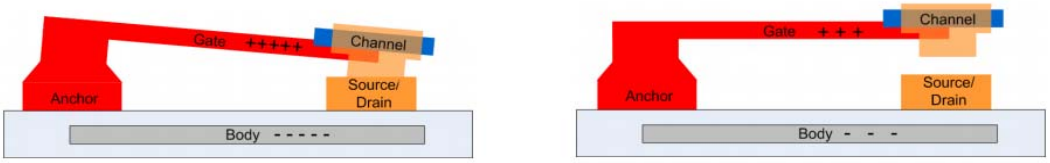
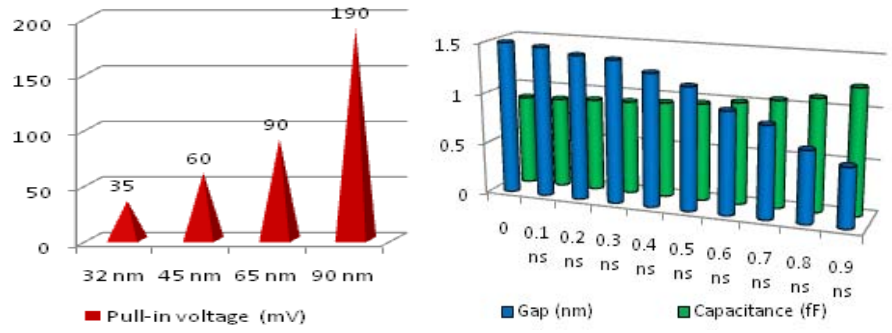



Fig. 2: (a) switch in the ON state (|Vgb|>Vpi), (b) switch in the OFF state (|Vgb|<Vpo)

- Case1: When (Vgb⩽Vpi) is applied, the electrostatic force of attraction between the opposite charges on the gate and body and the small Van der Waals force becomes large enough to pull the gate down. This stretches the springy coils and causes the gap between the gate and the body to decrease.
- Case2: When (Vgb⩾Vpi) i.e. with the voltage just exceeding the threshold voltage, the gap reduces to a critical value of 1/3 of initial gap and then the channel abruptly contacts the source/drain electrodes to form a conductive bridge for current to flow through the channel. The switch is said to be in the ON condition.
- Case3: When (Vgb⩽Vpo) i.e. with the voltage decreasing to a small value, the electrostatic force is reduced and eventually falls below the restoring force of the coils. This creates an air-gap that separates the channel from the source/drain electrodes thus preventing current flow through the switch. The switch is said to be in the OFF condition.

The pull-in voltage [10] applied between the gate and body for the given actuation pad dimensions is designed to be: Vpi $\alpha$ $g^{1.5}$, where 'g' is the gap thickness. It is observed from Fig.3 that Vpi decreases with technology scaling, leading to reduced power consumption. The simulation result in Fig.7 shows the change in input capacitance (important parameter for any switch) with time and that the switching time is about 1 ns.




(a) (b)

Fig. 3: (a) Nanorelay pull-in voltage for several standard technology nodes; (b) Gap between the cantilever and gate capacitance versus the switching time [1].

## 4. Fabrication Methodology

Nanorelay implementations can use processes that combine single-crystal materials and layered structures, thus permitting ultra small gaps needed for actuation. This allows electronics compatible voltages to be achieved at the expense of complex processes with high temperature deposition and selective removals.Nanorelays can be built using processes that were originally developed to make CMOS chips.

Step1: Firstly, the source, drain and body electrodes are formed by depositing a metallic material like 'tungsten' on top of an electrically insulating layer. Step2: A layer of removable, sacrificial material like 'silicon dioxide' is added to form the foundation of the movable electrode of the switch. The spots where the channel will make contact with the source and drain electrodes are etched away. Step3: A second layer of sacrificial material is deposited to crater a contoured surface. A metallic layer is then added to form the relay channel, its lowest points aligned with the source and drain electrodes. Step4: Another insulating layer is added to electrically isolate the channel from the next layer in the moving stack- the relay gate. This is built from a thick layer of semiconductor material, which is also used to form the spring like parts of the structure. An insulating layer on top protects the gate and springy coils as undesired material is etched away. Step5: 'Hydroflouric acidic vapor' is used to clear away the sacrificial material, leaving an air gap channel and the switch base. Despite additional mask layers in the fabrication process, nanorelays allow effective leakage reduction without the need for multi-threshold CMOS, which in turn saves mask layers.

## 5. Significance and Features of Nanorelays

### 5.1. Advantages

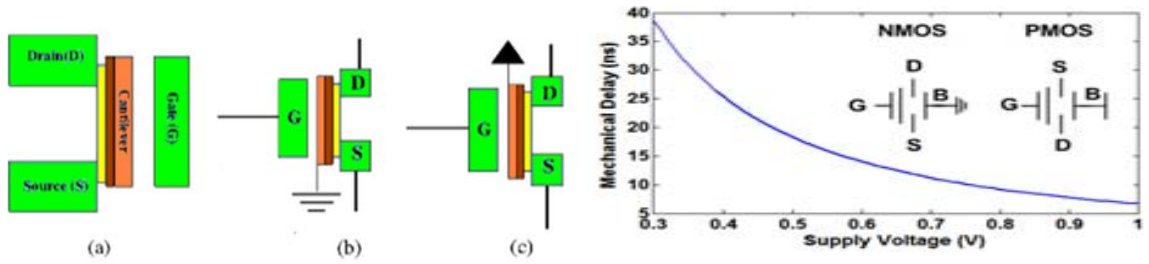
Since the leakage power will drop substantially, power gating using nanorelays could enable the use of low $V_T$ (threshold voltage) CMOS devices henceforth increasing the logic speed. Simulation results indicate that for the same lithographic dimensions, a nano-relay circuit will consume as little as 1/100th of the energy while occupying the same chip area as that of an equivalent CMOS circuit. Hence, these devices can be used as very efficient power-gating devices in order to improve the overall power consumption of a digital block when it is not in active operation. The mass of the movable electrode in a nano-relay is 1/10 grams, this means that accelerations upto 100000gs will be required to overcome the restoring force on the movable springs and accidentally cause the channel to come in contact with the source and drain electrodes. This clearly indicates that relay chips are least susceptible to vibrations and mechanical shock. The Switching delay is largely independent of electrical time constant. The electrical delay associated with charging and discharging a switch when the channel comes in contact with or is lifted off the source and drain is negligible compared to the mechanical switching time. Thus, we're free to use more wear and heat resistant materials like tungsten for the contacts thereby increasing the lifetime of these switches. This leads to the estimation that nanorelays can be used to make a practical microcontroller for an embedded sensor that switches a quadrillion ($10^6$) times without failing. This level of activity corresponds to running 1% of the time at speeds of 100MHz for 10 years. As relays are scaled down they're likely to become even more reliable as the input gate capacitance associated with the relay drastically decreases and so does the charging and discharging times. The outcome is that the heat dissipated via the contacts is minimized. Henceforth the cooling circuitry

hardware and cost is brought down by a great extent. It is even possible to make nano-relays fast enough to drive core logic in cell phones, tablets, smart cards, PDAs, wearable computers, pacemakers, defibrillators, multimedia, internet enabled appliances and other portable electronic gadgets that must not only be designed for fault tolerance but also for ULP consumption due to limited battery life. They are potentially relevant devices for low energy-exchange computing, low standby power and for dynamic or non-volatile configurability.

Due to "green-switch" properties such as zero leakage current, infinite sub-threshold slope, and temperature resilient behavior, nano-electromechanical switches (NEMS) are explored in this paper to mitigate the thermal reliability issues for 3-D integrated many-core memory-processor system. It is projected that nanorelay circuits made using mature 90nm chip technology can operate at speeds only upto 0.1GHz but the computing power capability is enough to drive the logic behind various sensors (pressure, flow, accelerometers) , cameras, implanted electronics (BioNEMS) and communication devices that will form the future. As nanorelays shrink, both their energy efficiency and speed will continue to improve, potentially upto a GHz or so.

## 5.2. Delay Reduction Techniques

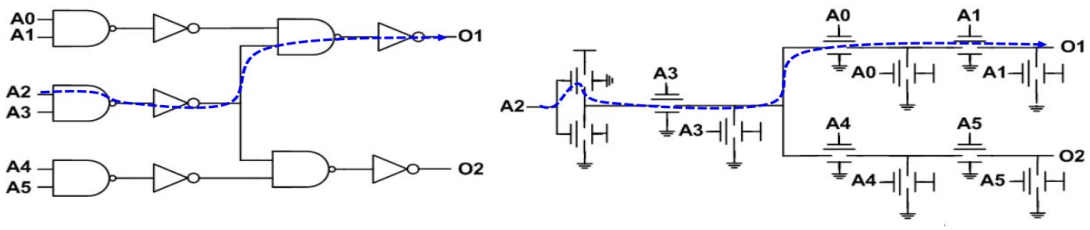
Nanorelays are the holy grail of digital electronics if they can be actuated at very high speeds; however, due to their mechanical nature, they posses high latency and so are not as fast as their counterpart modern CMOS devices; but what they lack in speed they make up for in energy efficiency.




(A) (B)

Fig. 4: (A)(a) Schematic of a four terminal NEMS device structure ; (b) P-NEMS device configuration; (c) N-NEMS device configuration[1].(B)Exponential dependence of mechanical delay on the supply voltage.

Method 1: The effect of long mechanical delays can be reduced by optimizing the digital circuit design. The best way to design a digital relay block is to arrange them into one single gate either in series or parallel instead of grouping them into discrete simple logic gates (each gate containing a small number of transistors as in CMOS design). This way all the nanorelays can be switched simultaneously resulting in a single mechanical delay for any operation performed. This technique is illustrated in Fig.9. This approach works as the delay associated with the movement of electrical signals through more complex circuits remains miniscule compared to the opening or closing of a single switch. An additional advantage of this approach is that circuits built this way need fewer devices to operate thus saving both chip space and cost. E.g. while a CMOS full adder cell requires 24 transistors, nanorelay adders need only 12 switches to perform the same operation.




(a) 4 Gate delays (b) 1 mechanical delay

Fig. 5: Comparison of CMOS v/s Nanorelay logic circuits by implementing a simple Boolean function. (a) CMOS: 30 transistors; (b) NEMS: 12 nanorelays.

Method 2: Another effective way to boost the speed is by reducing the inherent mechanical delay of the relays. This is practically realized by: (1) Use of light weight materials to fabricate the relay's gate/channel so that the switch can accelerate faster for the same actuation voltage. (2) Reducing the suspension gap between the gate and body so that the gate travels lesser distance between the on and off states of the switch. (3) Boosting the electrostatic force of attraction between the electrodes by applying a stronger electric field.

### 5.3. Field Programmable Gate Array

The basic FPGA architecture is composed of an array of Configurable Logic Blocks (CLBs), a programmable switch box for interconnection and I/O Pads. If the switch box is implemented using CMOS programmable switches as shown in Figure 6(b) then leakage current due to second order effects and large parasites causes the FPGA to consume more power and to operate at a lower clock frequency. These FPGAs are estimated [16] to be 3 times higher in total power consumption, 3 times larger in delay and 10 times less efficient in logic density than ASIC implementations. In FPGAs, leakage power accounts for nearly 20-25% of the total power dissipated in a 90nm CMOS [10] and increasingly more at smaller technology nodes. Out of this as much as 65% [10] of the total leakage is attributed to switches that route signals inside the FPGA. Upto 90% of FPGA area is dominated by programmable switches and routing resources. Nearly 60% of the total dynamic power dissipation in FPGAs is contributed by programmable routing switches which employ multistage buffers that drive one or more pass transistors in parallel. Each of these buffers is about 3 times larger than a pass transistor.

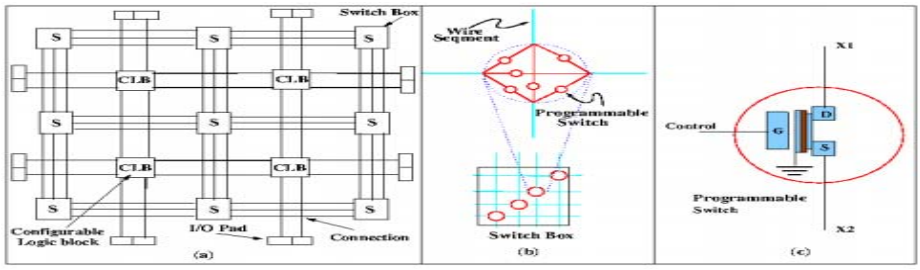



Fig. 6 [1]: (a) Simplified FPGA architecture consisting of, Configurable Logic Block (CLB), I/O Pads and Switch Blocks for routing; (b) Switch Box design and programmable switches; (c) A Programmable NEMS switch. When Control=0, X1 and X2 are connected and not when Control=1.

Integrating nano-relays into FPGA switch boxes and multiplexers will enable both power and complexity reduction. Nanorelays posses sizably lower parasitic capacitance and better driving strength; hence it can be successfully used to alter the fundamental tradeoffs between logic density, performance, energy consumption, speed and dynamic power consumption. These devices can be embedded in the power grid such that contacts are established by actuating the crossing wires. This will lead to removal of redundant switches and multipliers along with decreased routing complexity. A highly efficient architecture can be developed by integrating both CMOS and nanorelays into the FPGA architecture to function as logic blocks. The so obtained cFPGA (CMOS-Nanorelay FPGA) can nearly double the logic density and static leakage power improvement along with 30% dynamic power reduction as compared to the CMOS FPGA circuits. This performance improvement can be achieved by using 2T1N structures [1] as routing switches: Two CMOS transistors (2T): one for programming purpose and the other for signal transmission; one nanorelay (1N): the switching element.

## 6. Future Prospects

The biggest promise of NEMS technology is the development of extremely small sensor systems that can be used virtually everywhere and thus can impart intelligence to almost all man-made things. Reliable fabrication of various types of mechanical structures at this scale continues to be a challenge and packaging of these devices remains a much less investigated field. It has been demonstrated that memory and basic logic circuits like adders and multipliers can be built using nanorelays. Till date, high sensitivity gyroscopes and microphones, ultrasound transducers, microfluidics, lab-on-chip module, array feeds, phase shifters,

movable antennas, tunable capacitors and filters have been successfully realised using these nano devices. The least explored and upcoming area of NEMS application is in biomedical tools. The biomedical industry and especially society have much to gain from NEMS devices. These devices upon integration with CNT (Carbon Nano Tube) can be implemented in diagnostic tool/devices, biopharmaceuticals, implantable materials/devices and surgical aids. Results have shown their potential in controlling and monitoring critical mechanisms in various biomedical applications like flow sensors to replace batteries in pacemakers, barometric pressure sensors in kidney dialysis. They can also be used to provide precision fluid control in eye surgeries and to speed up the healing process in burn victims.

For the relays to become the next mainstream IC technology, the following developments take place: (1) Relays should shrink in size from the present μm scale to nm scale (2) They should be fabricated into much more complex systems (3) The next step would be to build a SOC like a microcontroller containing millions of switches (4) Develop optimization techniques to optimize the VLSI circuit designs (5) Get the wafer fabrication chain ready for those large chip designs. Realizing ICs containing millions of these nanorelays is relatively uncomplicated. Apart from some relay specific DRCs and device models, the same CAD tools developed for the silicon CMOS industry can be used to place and route relays and simulate its circuit behaviour. Software reuse is very critical since the process of rebuilding this infrastructure from scratch would be very expensive.

## 7. Conclusion

This paper presents the features, design and fabrication of suspended gate electrostatically actuated nanorelay. It emphasizes on its potential to mitigate several tradeoffs and issues associated with the continued usage of the current CMOS technology in chips. A comparison between the two technologies is made against various mechanical and electrical parameters like delay, power and area considerations to illustrate this point. Various delay minimization techniques are enlisted since reducing mechanical delays has been an upheld task that needs immediate attention. An important application of NEMS in FPGA routing switches is described to prove its relevance as an alternative device for leakage power reduction. Its adaptability with the current submicron CMOS processes and its wide range of applications in a variety of areas ranging from smart textiles to biomedicine makes nanorelays a versatile tool and marks the beginning of a new era in IC technology. Nanorelay appears to have the potential to break through the energy efficiency roadblock and restore the manifest destiny of electronics. Before long we may see high-end portable electronic gadgets that operate for weeks or even years on a single battery charge. All it takes is for a few million things to click into place.

## 8. Acknowledgement

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