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Design of Wideband Voltage Source Having Low Output Impedance, Flexible Gain and Controllable Feedback Current for EIT Systems

T R Qureshi [1, 2 +], C R Chatwin [1] and W Wang [1]

[1] Biomedical Engineering, University of Sussex, Brighton, UK
[2] COMSATS Institute of Information Technology, Islamabad, Pakistan

Abstract: The objective of this research is to establish a viable bandwidth envelope that can be used to design a constant EIT voltage source over a wide bandwidth having low output impedance for practical implementation. Electrical Impedance Tomography of the tissue can be performed by injecting current and measuring the resulting voltages, or by applying voltages and measuring the current developed. Interesting characteristics of breast tissues mostly lie above 1MHz; therefore a wideband excitation source covering higher frequencies (i.e. above 1MHz) is required. This research investigates a voltage controlled voltage source (VCVS), which can be used over a wide bandwidth (100Hz – 20MHz). A voltage source with user set gain and controllable feedback current is presented. This paper describes the performance of the designed EIT voltage source for different load conditions and load capacitances reporting signal-to-noise ratio, phase lag and output impedance of the source over the operational frequency range. Simulation data obtained using Pspice® is used to demonstrate the high-bandwidth performance of the source.

Keywords: Electrical impedance tomography, EIT, Impedance tomography hardware and voltage source.

1. Introduction

Electrical Impedance Tomography (EIT) systems require a wide range of frequencies for the measurement of voltage and current to be used to reconstruct conductivity and permittivity distributions in the body under investigation. Previous studies show that breast tissue characteristics may be best explored above 1MHz [1]. Therefore in order to study breast tissue characteristics an EIT system should at least extend measurements up to 10MHz to effectively characterize the breast [1]. EIT excitation can be performed by either injecting a current or applying a voltage. If currents are injected, then voltages on some or all electrodes are measured. If voltages are applied, then current through the active electrodes are measured [4]. EIT systems require applied and measured signals with high precision. Achieving high precision and high output impedance using a current source is difficult because it requires additional complex trimming circuits [2]. Precision is also degraded if we are dealing with a wide range of frequencies. In order to overcome the current source problems, a voltage source can be implemented using a broadband operational amplifier [4], [5], [6], [7]. Voltage sources with high precision are generally less costly and easier to implement. However, while designing a voltage source it is desirable to know the applied voltage and its resulting current. If a constant voltage drop is desired across a wide range of load impedances, then the voltage source should have low output impedance. This paper describes a voltage source design having current sensing capabilities with voltage gain and controllable feedback current. Depending upon the requirements, the voltage gain of the system is fixed and can be used to determine feedback current. The purpose of the feedback path is to control the current passing through the load. In this paper the bandwidth of the design is considered with the other performance parameters. The circuitry is designed to achieve a bandwidth of greater than 20MHz over a wide a range of loads in the presence of load capacitance and to

+ Corresponding author. Tel.: + 44 750 618 7973
E-mail address: t.r.qureshi@sussex.ac.uk

achieve as low output impedance as possible without any oscillation in the system at higher frequencies. Preliminary simulation results are generated to establish the bandwidth performance of the source.

2. Source Architecture

The suggested voltage source architecture is displayed in figure 1. This source has an ability to sense how much current is injected into the object and it can also control the maximum amount of current passing through the load (R_L). The current flowing through the load is limited by the feedback path. This source gives a voltage gain depending upon the requirements of the system.

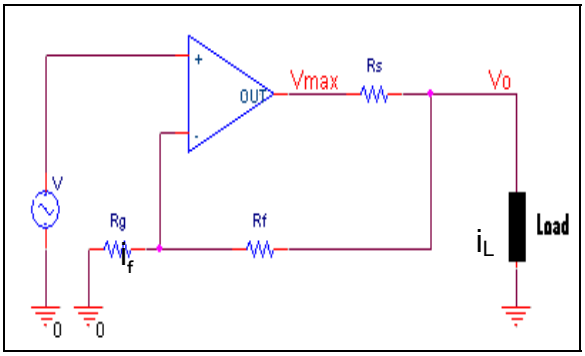

Figure 1: Single end source architecture

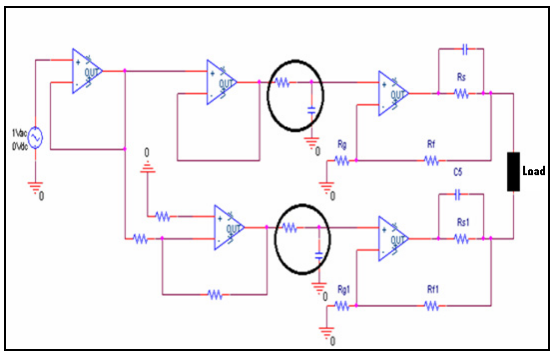

Figure 2: Differential source architecture

The output current for the operational amplifier is given by:

$$i_s = \left[\frac{(R_g + R_f) + R_L}{R_g R_L}\right] V_{in} \tag{1}$$

The maximum operational amplifier output voltage is given by:

$$V_{\max} = \left[\frac{R_S + R_L + (R_S + R_L)(R_g + R_f)}{R_g R_L}\right] V_{in} \tag{2}$$

Current passing through load depends upon the voltage gain of the system and can be expressed as:

$$i_L = \left[\frac{R_g + R_f}{R_g R_L}\right] V_{in} \tag{3}$$

3. Methodology

The circuit shown in figure 1 was simulated using Pspice® over a wide range of frequencies i.e. up to 1GHz. Wide bandwidth components were chosen to facilitate high frequency capabilities. System bandwidth limitations are mostly caused by amplifiers, therefore an amplifier with a gain bandwidth product greater than 100 MHz must be chosen to ensure high frequency capabilities. The device selected as a source is the OPA656 from Texas instruments whose unity gain bandwidth product is 500 MHz and can give 230 MHz gain bandwidth product with a gain of greater than 10. The minimum theoretical value of the load is decided and the circuit is tuned in such a manner that a constant voltage is dropped across the load with a maximum amount of current (i.e. 1mA) passing through the load. A differential amplifier is used across the sense resistor R_s to indirectly measure how much current is injected into the object. The op-amp output voltage varies with the change of the sense resistor R_s, as mentioned in equation 2. We need to specify certain parameters to find out the rest of the parameters in order to meet the design requirements. Firstly, the voltage gain of the system is set according to our requirement. The theoretical maximum current (i.e. 1mA) will pass through the load when the load becomes equal to the voltage gain. For this case that value of the load can be considered as the minimum value of load attached to the source having a maximum current of 1mA. As mentioned earlier, the maximum op amp voltage is dependent on R_s, so in order to keep the maximum op amp voltage according to its data sheet range we have fixed its maximum value in equation 2 to find the optimum value of R_s , which can be expressed as,

$$R_S = \frac{V_{\max} R_g R_L - (R_g + R_f) R_L V_{in}}{V_{in}(R_L + R_g + R_f)} \tag{4}$$

The gain of the system must not exceed the maximum op amp voltage. The circuit is tested in the presence of load capacitance and the results are shown in the following section.

4. Result and Discussion

The circuit is simulated to make a differential voltage source as shown in figure 2. The source is simulated with an ideal and non-ideal amplifier. The gain of the system is set to be 2.5. Theoretically, we know the value of maximum current to be injected. By knowing the voltage gain and injected current we may predict the load value. This load value can be the minimum condition to allow maximum current. Practically, a differential amplifier across the sense resistor gives the current injected to the load. Feedback current is fixed irrespective of load because of the fixed feedback resistors values. Therefore we can easily determine the Load current. Load values tested were 5k, 10k, 15k, 20k, 25k, 30k, 35k, 40k, 45k and 50k ohms in differential mode.

A single source signal is used to test the circuitry. In order to make a differential source, the generated signal is inverted using additional circuitry and both inverted and non-inverted signals are applied to the load simultaneously. (i.e. V^+ & V^-) as shown in figure 2. There is a slight difference in bandwidth of the individual voltage pulse (V^+ & V^-) when applied in differential mode. An additional RC circuit was used before the voltage source to minimize this difference and to control the oscillation in the system at higher frequency as highlighted in figure 2.

In order to minimize the difference in the bandwidth three possible cases were tested:

Case 1: Adding a non-inverting configuration in V^+ path instead of a simple buffer.

Case 2: Adjusting the values of the RC circuit until the difference become minimum.

Case 3: Removing the capacitor from the RC circuit.

Results show that only case 2 is helpful in minimizing the difference between the V^+ & V^-. Case 1 results in the increase of the magnitude and bandwidth of the signal. Case 3 also increase the bandwidth difference of V^+ & V^-.

To set a gain of 2.5 for the circuit shown in figures 1 & 2 we need to specify feedback resistor values. Suppose the value of R_g is fixed. Depending upon the predefined gain of the circuit, R_f can be calculated as:

$$R_f = (Gain - 1)R_g$$

The circuit is simulated for the above gain and group of loads without load capacitance. The circuit is also simulated in the presence of load capacitances: 10pF, 30pF, 50pF and 100pF. The simulation results show that in the presence of load capacitance the circuit shows some oscillation at higher frequencies i.e. above 5MHz. In order to control this an additional capacitor is added in parallel with the sense resistor as shown in figure 2. Results show that the bandwidth of the circuit not only remains stable with the increase in load but also increases with the decrease in load capacitance. Simulation results with load capacitance 30pF and 100pF are shown in figure 3 and 4 respectively.

The bandwidth using an ideal device is limited by the cut off value of the RC circuit. This cut off value is used to remove the oscillation in the system at higher frequencies and to minimize the difference in the bandwidth of V^+ & V^- . Results show that by adjusting the RC circuit values the difference can be minimized to approx less than 1%. The bandwidth difference is reported in the table 3 & 4. Results show that the bandwidth achieved without load capacitance and having a high load capacitance i.e. 10pF is almost the same. If load capacitance is decreased higher bandwidth can be achieved. The average bandwidth achieved with no load capacitance, 10pF, 30pF, 50pF and 100pF load capacitance are 21 MHz, 20.82 MHz, 22.21 MHz, 23.45 MHz and 26.31 MHz respectively. The bandwidth achieved using different loads are shown in Table 5. The bandwidth achieved in the table 5 is the -3db point of the original signal. Ryan Halter [3] reported an EIT system which can achieve a system bandwidth between 10 – 12.5 MHz. If the design is fabricated with high accuracy and precision then the design will have less effect from stray capacitance. As a result a wider bandwidth system greater than 12 MHz can be achieved.

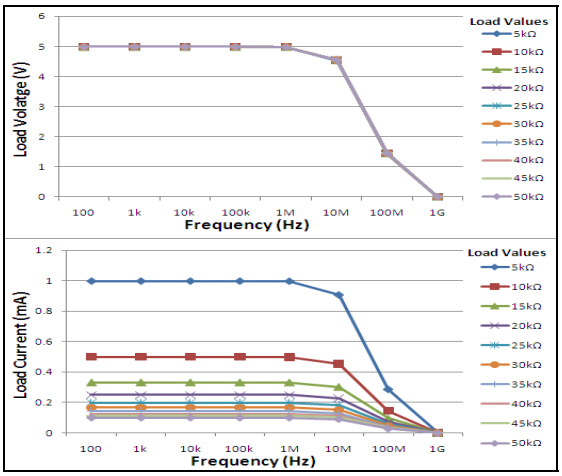

Figure 3: Load voltage and current versus frequency using a 30pF load capacitance

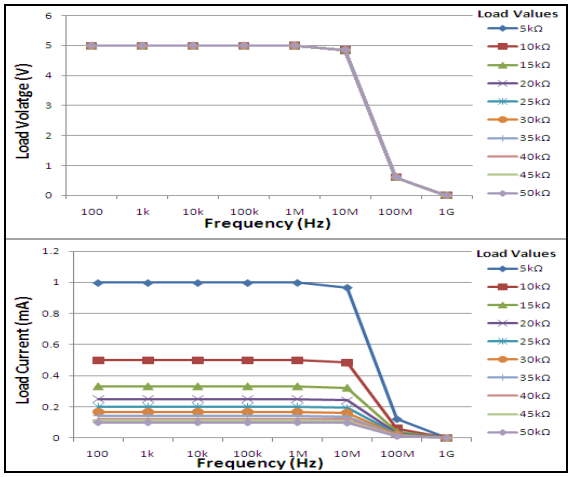

Figure 4: Load voltage and current versus frequency using a 100pF load capacitance

Signal phase is shown in figure 5. The results show that there is phase difference of approx -3˚ to -62˚ across the whole range of tested load for a positive terminal output voltage and a phase difference of approx 180˚ to 113˚ with a negative terminal output voltage. Signal phase is the phase difference between the input and output signal. Phase difference is very small until 1MHz and increases above this frequency. Detailed phase difference results are reported in Table 1.

Signal-to-noise (SNR) remains within defined limits for different values of loads and load capacitance. The voltage SNR is for a 2.5V signal and is approximately between 127dB to 80dB for V^+ & V^- signal as shown in figure 6. SNR is calculated using Pspice® Noise analysis functions. The total noise contribution at each frequency is calculated using Pspice®. Probes are used to measure the total RMS noise across the band. Signal-to-noise ratio is determined from equation 5. Ryan Halter [6] claims a SNR of greater then 94dB up to 2 MHz, 90dB up to 7 MHz and 65dB at 10 MHz. According to our findings a SNR of 101 dB up to 1 MHz and between 101 to 90 dB up to 10 MHz can be achieved by building good quality printed circuit boards and by minimizing the on board parasitic impedances. Detailed SNR is reported in Table 2.

$$SNR = 20\log_{10}\left(\frac{Signal}{Total\ noise}\right) \tag{5}$$

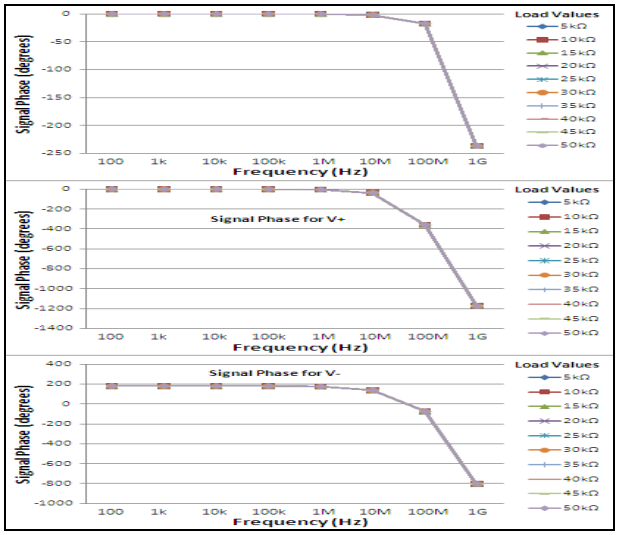

Figure 5: Output Voltage phase difference

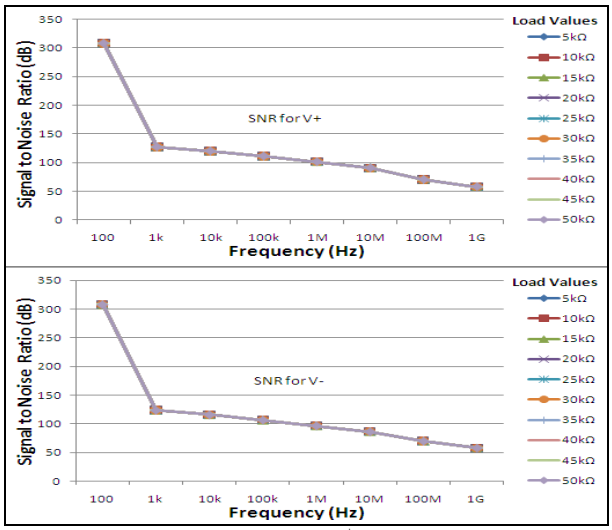

Figure 6: SNR for V^+ and V^- signal

Ideally, the voltage source should have zero output impedance. Practically it is not possible to have zero output impedance but to get better performance it should be as low as possible. The circuit has been simulated to evaluate the output impedance for various frequencies. The results show that output impedance varies between approx 13Ω to 4.75kΩ. The entire circuit is converted into its Thevenin's equivalent and the

output impedance / resistance and can be determined using the voltage divider rule as shown in equation 6. The detailed output impedance is reported in Table 6.

$$Z_{out} = \frac{Z_{Load} V_{in} - V_{Load} Z_{Load}}{Z_{Load}} \quad (6)$$

Table 1: Phase Difference of Input vs Output voltage at 5kΩ and 30kΩ load with 30pF load capacitance

Frequency (Hz)	V+		V-	
	Input	Output	Input	Output
100k	0˚	0˚	0˚	179.61˚
1M	0˚	-3.55˚	0˚	176.08˚
10M	-1.70˚	-35˚	-1.70˚	142.17˚
20M	-3.41˚	-62˚	-3.41˚	113˚

Table 2: SNR for voltage source with 30pF load capacitance

Frequency (Hz)	SNR (dB)	
	V^+	V^-
1k - 100k	127 – 110	123 – 106
100k – 1M	110 – 101	106 – 96
1M – 10M	101 – 90	96 – 86
10M – 30M	90 – 83	86 – 80

Table 3: Bandwidth difference of voltage signal with 30pF load capacitance

Load (Ω)	Bandwidth (MHz)		Difference (%age)
	V+	V-	
5k	22.18	22.00	<1% approx
10k	22.31	22.13	<1% approx
15k	22.35	22.17	<1% approx
20k	22.37	22.19	<1% approx
25k	22.37	22.20	<1% approx
30k	22.39	22.21	<1% approx
35k	22.39	22.21	<1% approx
40k	22.40	22.22	<1% approx
45k	22.40	22.22	<1% approx
50k	22.40	22.22	<1% approx

Table 4: Bandwidth difference of voltage signal with 50pF load capacitance

Load (Ω)	Bandwidth (MHz)		Difference (%age)
	V+	V-	
5k	23.18	23.47	1.3% approx
10k	23.30	23.61	1.3% approx
15k	23.35	23.66	1.3% approx
20k	23.37	23.68	1.3% approx
25k	23.38	23.69	1.3% approx
30k	23.39	23.70	1.3% approx
35k	23.39	23.71	1.3% approx
40k	23.40	23.71	1.3% approx
45k	23.40	23.72	1.3% approx
50k	23.41	23.72	1.3% approx

Table 5: Load voltage bandwidth at corresponding loads

Load (Ω)	Bandwidth (MHz)					
	Ideal Device	Non Ideal Device				
		No Load Capacitance	Load Capacitance (pF)			
			10	30	50	100
5k	31.76	21	20.69	22.04	23.26	26.16
10k	31.76	21	20.80	22.16	23.39	26.27
15k	31.76	21	20.83	22.20	23.43	26.30
20k	31.76	21	20.85	22.22	23.45	26.32
25k	31.76	21	20.86	22.24	23.47	26.33
30k	31.76	21	20.87	22.24	23.48	26.34
35k	31.76	21	20.87	22.25	23.48	26.34
40k	31.76	21	20.88	22.25	23.49	26.34
45k	31.76	21	20.88	22.25	23.49	26.35
50k	31.76	21	20.88	22.25	23.49	26.35

Table 6: Output impedance for voltage source parallel with 30pF load capacitance

Load (Ω)	Output Impedance (Ω)		
	100kHz	1MHz	10MHz
	13.23	16.86	492.57
10k	25.67	32.51	965.39
15k	37.90	48.15	1.44k
20k	50.53	64.21	1.91k
25k	63.16	80.26	2.38k
30k	75.79	96.31	2.86k
35k	88.42	112.36	3.33k
40k	101.05	128.41	3.80k
45k	113.69	144.46	4.28k
50k	126.32	160.51	4.75k

5. Conclusion

In this paper a voltage controlled voltage source (VCVS) has been simulated with a non-ideal operational amplifier for the Electrical impedance tomography (EIT) system. The source architecture has been presented. Theoretical equations showing the behavior of the circuit are described. Circuit parameters have been defined according to the requirements specification. The source has been simulated over a wide band of frequencies with and without the presence of load capacitance. Other performance parameters like output impedance, Signal-to-noise ratio, Magnitude and signal phase lag are also reported. Efforts have been made to increase the bandwidth of the source and have achieved a bandwidth of greater than 20MHz. The source has achieved low output impedance with an acceptable level of SNR.

6. References

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