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DC Characteristic Analysis of Single-Electron Transistor Based on MIB Model

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***Abstract*— DC characteristic of the single-electron transistor (SET) in various physical parameters are analyzed based on Mahapatra-Ionescu-Banerjee (MIB) model. To the best of our knowledge this work has been done for the first time. It is shown that for SET by increase of the channel width and the length of both the side gate and the control gate, the Coulomb blockade region becomes narrower and the oscillation period of the drain current decreases. Also it indicates that increase of the oxide thickness of both the side gate and the control gate cause the Coulomb blocked region to become wider and the oscillation period of the drain current to increase. In addition, it is illustrated that increase of the channel thickness causes the Coulomb blocked region to become a bit narrower but the oscillation period of the drain current to remain constant.**

Keywords-single electron transistor; Coulomb blockade; drain current.

I. INTRODUCTION

With the development of the modern data processing systems, integrated circuits have been developing to nanoscale circuits. The continues minimizing in scaling of the current semiconductor LSI technology causes serious problems, including interconnect delays, increasing power consumption, limited integration density, and device scaling constraints [1], [2]. Utilizing nanodevices like single electron transistor (SET) is an important method to solve these problems. SET has attracted much attention because of its nano feature size [3], ultra low power dissipation [4], [5], new functionalities [6], and unique electronic characteristics [7]. SET is based on the Coulomb blockade of tunneling. For a bias voltage less than threshold limit due to the charges' Coulomb repulsive force effect, the Coulomb blockade prevents flow of the current through tunnel junction.

Typical metal-film SET includes a small metal island connected to the external circuits with two tunnel junctions and a gate capacitive coupled to the island. The basic schematic of a SET device is depicted in Fig. 1. SET consist of five main parameters including source tunnel junction capacitance and resistance (C_S and R_S), drain tunnel junction capacitance and resistance (C_D and R_D), and side gate capacitance (C_G). It is possible that the second gate connects to the island which is so called control gate capacitance (C_C).

For proper operation of a SET, two fundamental conditions should be prepared. Firstly, to avoid an unwanted tunneling which is the result of the thermal energy, it is necessary to have the total capacitance of the island, C, as small as the charging energy, $E_C=e^2/2C$, to be much larger than the thermal energy, k_BT. Secondary, with regard to the uncertainty principle the resistance of the tunneling barriers need to exceed the quantum resistance $R=h/e^2\approx 26\ \text{k}\Omega$ [8]. If these conditions are satisfied, the number of the electrons on the island becomes fixed, and more energy is needed to add an extra electron to the island.

In a SET, for instance, where source and control gate terminals have been grounded, and drain and side gate terminals have been biased at V_{DS} and V_{GS} respectively, the tunneling current (I_{DS}) through the SET changes periodically as a function of the applied side gate voltage with a period of e/C_G which both V_{GS} and V_{DS} can control it. The I_{DS} versus V_{GS} characteristic of the SET is illustrated in Fig. 2. The region where the I_{DS} is almost zero is known as the Coulomb blockade region. For digital operations, SET should be biased in such a manner that $V_{DS}<e/C$, otherwise there is no Coulomb blockade region in SET characteristics. Here, C is sum of C_G, C_S, and C_D.

The first compact model for SET devices has been proposed by Uchida et al. [9]. This model uses master equation (ME) method and is limited to $|V_{DS}|<e/C$ so this model is merely applicable for digital circuits design. It could not explain the device asymmetry effect and does not account the background effect which is significant for SET operation. Inokawa et al. [10] have extended Uchidas' model to the asymmetric devices and also have included the background charge effect. However, the model is still limited to $|V_{DS}|<e/C$. Le Royer et al. [11], and G.Lientschnig et al. [12] have proposed ME-based models which are quite accurate and valid for $|V_{DS}|>e/C$. However, these models are time consuming for large circuit simulations. Other model is MIB [13] model (named after the developers, Mahapatra, Ionescu, and Banerjee). MIB had used ME method to develop their model. This model is limited to $|V_{DS}|<3e/C$, therefore applicable for digital and analog circuits design. Moreover this model presents a simple efficient method to extract the model parameters for a generalized asymmetric device which is essential for SET-based circuit design [14]. In this paper, we are using MIB model to show the behavior of SET and HSPICE simulator for simulation propose.

The remainder of the paper is organized as following; in section II, the effect of variations in physical parameters of silicon-based dual-gate SET on its I_{DS}-V_{GS} characteristic has been analyzed theoretically. In section III, simulation results have been shown.

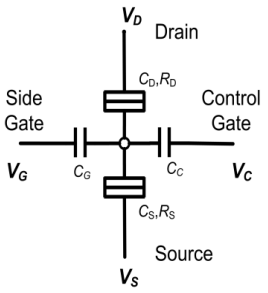

Figure 1. The SET schematice

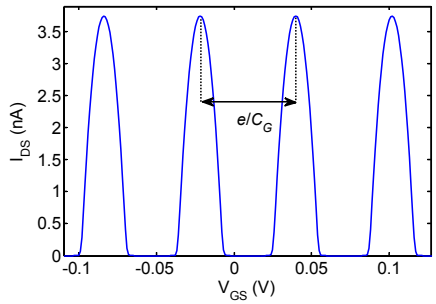

Figure 2. I_{DS} versus V_{GS} characteristic of SET

II. THEORETICAL ANALYSIS

A. Helmholtz Free Energy for SET

The energy which determines electrons transportation through a single-electron device is Helmholtz free energy which is defined as difference between total energy stored in the device and the work done by power source. Total energy stored includes all of energy components when an island is charged with an electron. For a SET with source and control gate terminals grounded, and drain and side gate terminals biased at V_{DS} and V_{GS}, the free energy has been formulated as following:

$$F = E - Q_D V_{DS} - Q_G V_{GS} \tag{1}$$

Here E is the electrostatic energy, Q_G is the charge of the side gate capacitance, and Q_D is the charge at drain tunnel junction capacitance. The change of Helmholtz free energy is calculated as:

$$\Delta F = F_f - F_i \tag{2}$$

Where F_i and F_f are the Helmholtz free energy of the system before and after an electron tunneling happens, respectively. A tunneling could only happen if ΔF is negative. For a logic operation, i.e., when the number of the electrons in the island is 0 or 1, ΔF is defined as following [14]:

If an electron tunnels from the source terminal to the island, ΔF is defined as:

$$\Delta F = \frac{C_D}{C} V_{DS} + \frac{C_G}{C} V_{GS} < 0 \tag{3}$$

For the electron tunneling of the island to the source terminal, ΔF is:

$$\Delta F = -\frac{C_D}{C} V_{DS} - \frac{C_G}{C} V_{GS} < 0 \tag{4}$$

If an electron tunnels from the island to the drain terminal, ΔF is defined as:

$$\Delta F = \frac{(C_S + C_G + C_C)}{C} V_{DS} - \frac{C_G}{C} V_{GS} < 0 \tag{5}$$

For the electron tunneling of the drain terminal to the island, ΔF is:

$$\Delta F = \frac{(C_S + C_G + C_C)}{C} V_{DS} - \frac{C_G}{C} V_{GS} < 0 \tag{6}$$

B. Stability Plot for SET

In SET, V_{DS} versus V_{GS} characteristic is known as stability plot. The stability plot of the SET is obtained with setting equations (3-6) equal to zero, thus the four lines' equation will be obtained so that their cross create a rhombus. Slop of these lines has been formulated as following:

If an electron tunnels from the island to the drain terminal and vice versa, lines' slop is obtained as:

$$S_1 = \frac{C_G}{C_S + C_G + C_C} \tag{7}$$

If an electron tunnels from the source terminal to the island and vice versa, lines' slop is achieved as:

$$S_2 = -\frac{C_G}{C_D} \tag{8}$$

The stability plot of the SET is illustrated in Fig. 3. In this Figure the rhombus outside regions corresponded to stable regions with an integer number of the excess electrons on the island. In rhombus inside, there is no excess electron on the island (the Coulomb Blocked region). For logic operation, if V_{GS} is increased and V_{DS} is kept constant below the Coulomb blockade, $|V_{DS}|<e/C$, (which is equivalent to a cut through the stable regions in the stability plot, parallel to the V_{GS}-axis) the current will oscillate with the period of e/C_G.

C. Fabrication Parameters of SET

The basic structure of silicon-based dual-gate SET is shown in Fig. 4. The main fabrication parameters are source and drain tunnel junction capacitances, side gate capacitance, and control gate capacitance. These parameters are formulated as following [15]:

$$C_G = \varepsilon_{SiO_2} \frac{L_G W_{ch}}{T_{Gox}} \tag{9}$$

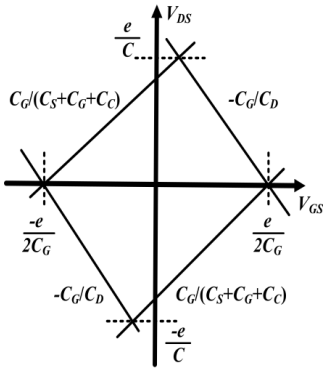

Figure 3. Stability plot for the SET

Where C_G, L_G, W_{ch}, and T_{Gox} are side gate capacitance, side gate length, channel width, and side gate oxide thickness, respectively.

$$C_C = \varepsilon_{SiO_2} \frac{L_C W_{ch}}{T_{Cox}} \tag{10}$$

Where C_C, L_C, and T_{Cox} are control gate capacitance, control gate length, and control gate oxide thickness, respectively.

Before any electron tunneling, the tunneling junctions act as capacitances so it could be written as:

$$C_S = C_D = \varepsilon_{Si} \frac{T_{Si} W_{ch}}{L_G} \tag{11}$$

Where C_S, C_D, and T_{Si} are source capacitance, drain capacitance, and channel thickness, respectively.

D. Calculation of Drain Current for the SET

For the digital operation, MIB model is written as following [13]:

$$I_{DS} = \lambda \frac{I_S(0) I_D(1)}{I_S(0) + I_D(1)} \tag{12}$$

Where $I_S(0)$ and $I_D(1)$ (the digit inside each parenthesis indicates the number of electrons in island) are tunneling currents from the source terminal to the island and from the island to the drain terminal respectively, which is represented as following:

$$I_S(0) = \frac{\lambda V_{island} - \alpha}{\left[1 - \exp\left(\frac{\lambda V_{island} - \alpha}{V_T}\right)\right] R_S} \tag{13}$$

$$I_D(1) = \frac{\lambda V_{DS} - \lambda V_{island} + \alpha}{\left[1 - \exp\left(\frac{\lambda V_{DS} - \lambda V_{island} + \alpha}{V_T}\right)\right] R_D} \tag{14}$$

TABLE I. DESCRIPTION OF THE SET NANODAMASCENE PROCESS VARIABLES.

Description	Value
W_{ch}	15nm
L_G	20nm
L_C	10nm
T_{Cox}	10nm
T_{Gox}	5nm
T_{Si}	15nm

Here λ holds the sign of V_{DS} and the box function, [], returns the greatest integer less than or equal to its term. Also α is $e/2C$ and for V_{island} we have:

$$V_{island} = \frac{C_D}{C} V_{DS} + \frac{C_G}{C} V_{GS} \tag{15}$$

III. SIMULATION RESULTS

Table I represents the value of the parameters that is used for the fabrication of the silicon-based dual-gate SET [16]. In all simulations it is assumed that V_{DS} = 0.15 mV and T=2 K.

Fig. 5 illustrates the channel width variation effect on the I_{DS}-V_{GS} characteristic of SET. It is shown that, by increase of the channel width, the Coulomb blocked region becomes narrower and the oscillation period of the drain current decreases. These results conform to the theoretical discussions of the section II. This is because by increase of the channel width, all capacitances change but the slope of S_2 remains constant and the slope of S_1 reduces, so rhombus inside area or the Coulomb blocked region decreases. In addition, the side gate capacitance becomes less, therefore the oscillation period of the drain current decreases.

Fig. 6 introduces the side gate length variation effect on the I_{DS}-V_{GS} characteristic of the SET. It is demonstrated that, the increase of the side gate length causes the Coulomb blocked region to become narrower and the oscillation period of the drain current to become less. According to the equations (9-11), by increase of the side gate length, all capacitances are changed but the slope of S_2 remains constant and the slope of S_1 reduces, so the Coulomb blocked region decreases. The variation effect in the side gate length is less than the variation effect in the channel width.

Fig. 7 demonstrates the channel thickness variation effect on the I_{DS}-V_{GS} characteristic. It is illustrated that, by variation of this parameter, the oscillation period of the drain current remains constant. Besides, it is observed that if the channel thickness increases, the Coulomb blocked region becomes wider and vice versa. The variation effect in the channel thickness is small because considering section II, it is

observed in the slope equations of all lines that specify the Coulomb blocked region.

Fig. 8 illustrates the control gate length variation effect on the I_{DS}-V_{GS} characteristic. It is shown that, the increase of the control gate length causes the Coulomb blocked region to become narrower and the oscillation period of the drain current to decrease.

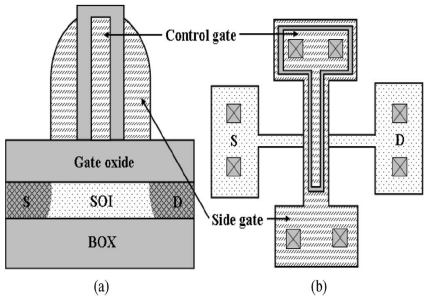

Figure 4. (a) Structure and (b) top view of the fabricated SET.

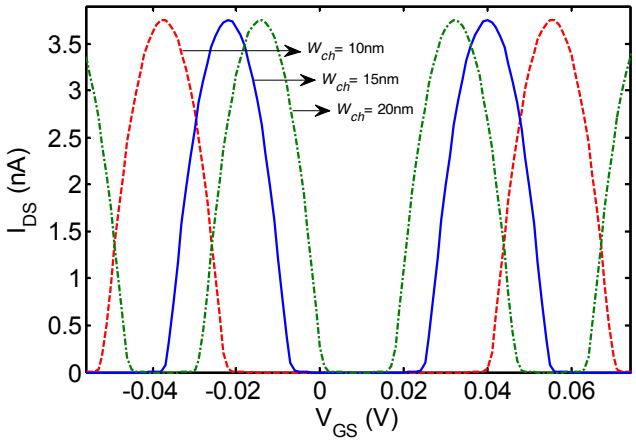

Figure 5. Variation effect in the channel width on the I_{DS}-V_{GS} characteristic of the SET.

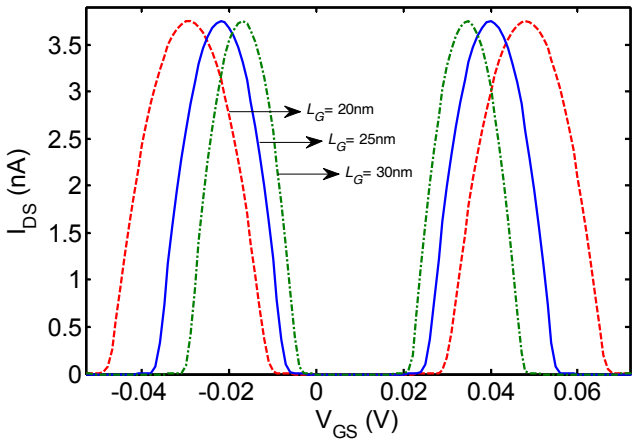

Figure 6. Variation effect in the side gate length on the I_{DS}-V_{GS} characteristic of the SET.

Fig. 9 shows the variation effect of the side gate oxide thickness on the I_{DS}-V_{GS} characteristic. It is demonstrated that, by increase of the side gate oxide thickness, the Coulomb blocked region becomes widder and the oscillation period of the drain current increases. According to section II, increase of this parameter causes the side gate capacitance to become less and the slope of both S_1 and S_2 to increase. Furthermore, by increase of the side gate oxid thichness, the control of gate voltage on the drain current is increased.

Fig. 10 introduces the variation effect of the control gate oxide thickness on the I_{DS}-V_{GS} characteristic. It is shown that, the increase of the control gate oxide thickness causes the Coulomb blocked region to become wider and the oscillation period of the drain current to increase.

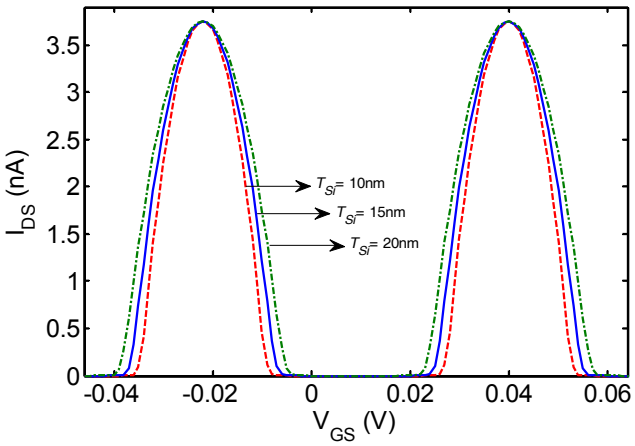

Figure 7. Variation effect in the channel thickness on the I_{DS}-V_{GS} characteristic of the SET.

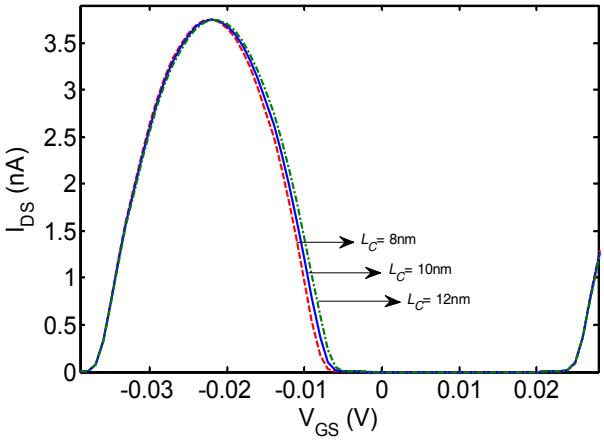

Figure 8. Variation effect in the control gate length on the I_{DS}-V_{GS} characteristic of the SET.

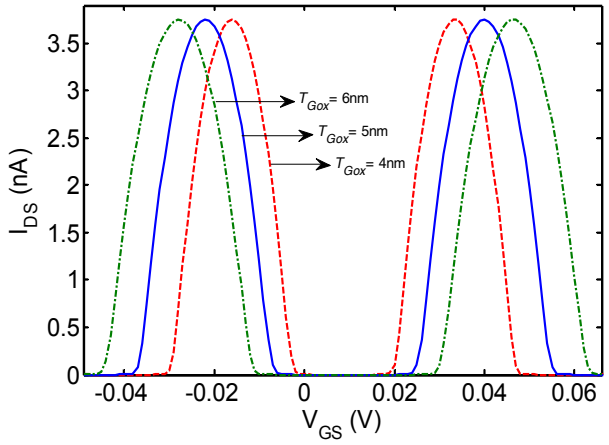

Figure 9. Variation effect in the side gate oxide thickness on the I_{DS}-V_{GS} characteristic of the SET

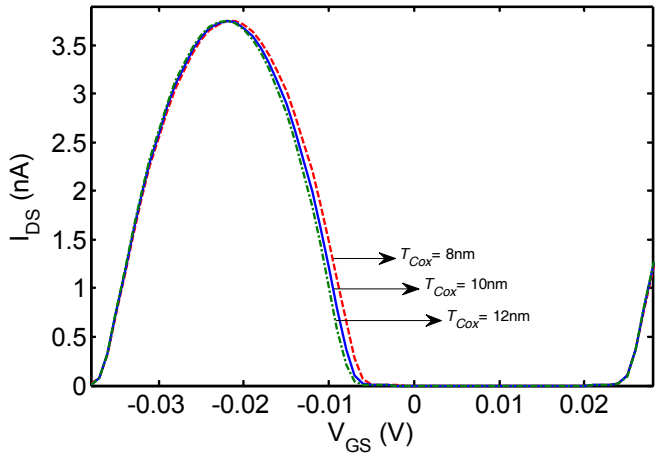

Figure 10. Variation effect in the control gate oxide thickness on the I_{DS}-V_{GS} characteristic of the SET.

IV. CONCLUSION

We analyzed DC characteristic of the SET in various physical parameters based on MIB model. At the first step, we grounded the source and the control gate terminals of the SET and biased the drain and the side gate terminals at V_{DS} and V_{GS}, respectively. Then for the observation of the physical parameters variation effects on the SET characteristic, we increased four parameters including the channel width, the side gate and the control gate lengths, and the control gate oxide thickness individually; consequently, it is observed that the Coulomb blockade region becomes narrower and the oscillation period of the drain current decreases. Moreover, we increased the oxide thickness of both the side gate and the control gate and witnessed that the increase of the above mentioned parameters result the Coulomb blocked region to become wider and the oscillation period of the drain current to increase. In addition, we increased the channel thickness and noticed that the Coulomb blocked region becomes slightly narrower but the oscillation period of the drain current remains almost constant. The Effects of all mentioned parameters on the SET characteristic are simulated by HSPICE simulator.

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